REMARKS

Reconsideration of the patent application in view of the preceding amendments and the following remarks is respectfully requested. Claims 28, 52, and 54 are currently amended, and claims 29, 53, 55, and 56 will be cancelled upon entry of this Amendment.

I. Rejection of the Claims Under 35 U.S.C. § 102

In the office action dated January 2, 2003 the Examiner rejected claims 28, 52 and 54 under 35 U.S.C. § 102. The Examiner stated that the claimed invention was anticipated by Scepanovic, U.S. Patent No. 5,914,887. Applicants respectfully disagree with the Examiner's rejection and contend that Scepanovic does not disclose every element of Applicants' invention. To expedite prosecution, however, Applicants have cancelled claims 28, 52, and 54 without prejudice, thereby rendering the Examiner's rejection moot. Applicants specifically reserve the right to pursue the subject matter of claims 28, 52 and 54 in a continuation application or other related case.

II. Allowable Subject Matter

In the office action dated January 2, 2003, the Examiner objected to claims 29-35, 53, 55 and 56 as being dependent upon a rejected base claim. Applicants, in response, have currently amended each of the base claims—28, 52, and 54—such that they now contain the limitations of claims 29, 53, 55 and 56 respectively. Accordingly, Applicants respectfully submit that all claims pending after entry of this Amendment are in condition for allowance.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

28. (Currently amended) For a placer that places circuit modules in integrated-circuit ("IC") layouts, the placer using a set of partitioning lines, that define a plurality of slots, to partition an IC layout region into a plurality of sub-regions corresponding to said slots, a method of pre-computing costs of placing circuit modules in an IC-layout region, the method comprising:

a) selecting a first group of said slots;

b) computing a first attribute of a set of one or more interconnect lines necessary for connecting the first group of said slots, wherein computing the first attribute comprises calculating the length of said set of interconnect lines;

c) computing a second attribute of the set of interconnect lines;

d) storing the computed attributes in a storage structure.

Claim 29 (cancelled)

52. (Currently Amended) A method of placing circuit modules in a region of

an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net,

d) retrieving from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions;

e) computing a placement cost of said net within said region by using the retrieved attributes;

f) changing the position of a circuit element of the net from one sub-region to another;

g) identifying a new set of sub-regions that contain the circuit elements of the net;

h) retrieving multiple pre-computed attributes of a different set of

interconnect lines necessary for connecting the identified new set of sub-regions; and.

i) computing a new placement cost of said net within said region by using the attributes retrieved for the different set of interconnect lines.

Claim 53 (cancelled)

54. (New) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC-layout region into several sub-regions;

b) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net,

c) for each particular net, retrieving multiple pre-computed attributes of a connection graph that models the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net, wherein the connection graph is either a Steiner tree or a minimum spanning tree;

d) computing a placement cost for the IC layout within said region by using the retrieved attributes.

Claim 55 (cancelled)

Claim 56 (cancelled)